

Electronics & ICT Academy IIT Roorkee



An Initiative of Ministry of Electronics & Information Technology (MeitY) Government of India

Joint Faculty Development Program

on

VLSI Design using Open source tools

Two - Week Joint Faculty Development Programme In association with



Feb 10 – Feb 21, 2025 02:00 PM – 06:00 PM Everyday

Register Before: Feb 7, 2025

Mode of Delivery is Online



About E&ICT Academy

Electronics and ICT Academy is an initiative of Ministry of Electronics & Information Technology (MeitY), Govt. of India for conducting various Faculty/ Research Scholar Development Programme. Academy has planned short-term training programs on fundamental and advanced topics in IT, Electronics & Communication, Product Design, and Manufacturing with hands-on training and project work using the latest software tools and systems. In addition, the Academy will conduct specialized/customized training programs and research promotion workshops for corporate sector & educational institutions.

Prerequisites

No experience is required, but fundamental knowledge of any programming language would be helpful.

Objectives of the course

- Introduce participants to the complete VLSI design flow, covering high-level and physical design aspects.
- Enable participants to use high-level synthesis tools like Intel HLS Compiler for system integration and SoC design.
- Familiarize learners with logic and sequential circuit optimization techniques for efficient design implementation.
- Develop skills in physical design processes, including placement, routing, and power planning.
- Provide an in-depth understanding of advanced verification techniques, such as DRC, LVS, and extraction.
- Equip participants with low-power design methodologies

Focus Areas

- Introduction to VLSI Design Flow
- High-Level Synthesis (HLS)
- Logic and Sequential Circuit Optimization
- Physical Design:
- Advanced Verification Techniques
- Low Power Design: Techniques for optimizing power efficiency in VLSI design.

Course Features

- 40 Hours of Lectures, hands-on, and Pedagogy/Industry sessions.
- Lectures from Expert Speakers, Hands-on from industry/Academia experts.
- Access to learning material and video lectures
- Certificate by E&ICT Academy IIT Roorkee

Course Outcomes

Participants are likely to:

- Understand and implement the VLSI design flow, from high-level synthesis to physical design.
- Use Intel HLS Compiler to design and integrate systems on Intel SoC FPGAs.
- Apply optimization techniques for logic synthesis, sequential circuits, and FSMs to improve design efficiency.
- Perform physical design tasks such as partitioning, placement, floor planning, and routing with practical understanding.
- Conduct advanced verification processes, including delay calculations, DRC, LVS, and extraction, to ensure design integrity.



Experts from Academia/Industry

Who Should Register?

Any Interested Faculty/PhD-Scholars UG/PG/ & Industry Persons can register

Registration Fee

Fees: ₹ 500/- Faculty/Research Scholar Note: Registration Fee is Refundable if the cancellation request is submitted before the last date of registration.

How to make Payment

Please make the payment first using the below link upload the payment receipt when filling out the Google registration form

https://eict.iitr.ac.in/instruction-for-payment/

Conference Code: EICTIITR-FDP-25-27

Registration Link

https://forms.gle/5nxKUbL4g2T8gqUk6



Scan QR for registration

Register before: Feb , 2025

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Resourse Person

• experts from IITs/NITs / IIITs and Industry experts

Principal Coordinator

Prof. Gaurav Trivedi, IIT Guwahati

Joint Principal Coordinators

- Prof. Sanjeev Manhas, IIT Roorkee
- Anand Bulusu, IIT Roorkee
- Prof. Lava Bhargava, MNIT Jaipur
- Dr. Sangeeta Singh, NIT Patna
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