eict
IIT Roorkee

Electronics & ICT Academy IIT Roorkee

An Initiative of
Ministry of Electronics & Information Technology (MeitY)
Government of India

A Joint Faculty Developmet Programme on

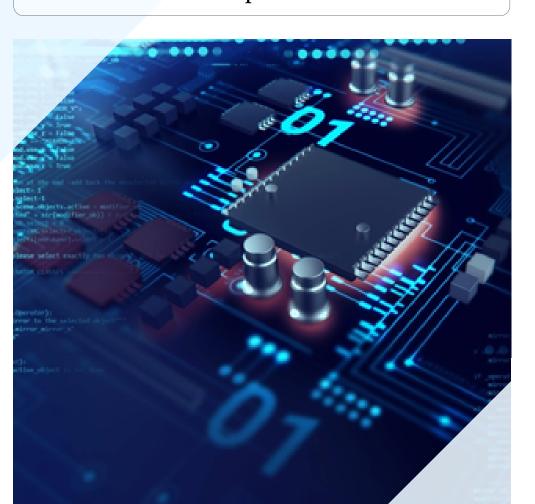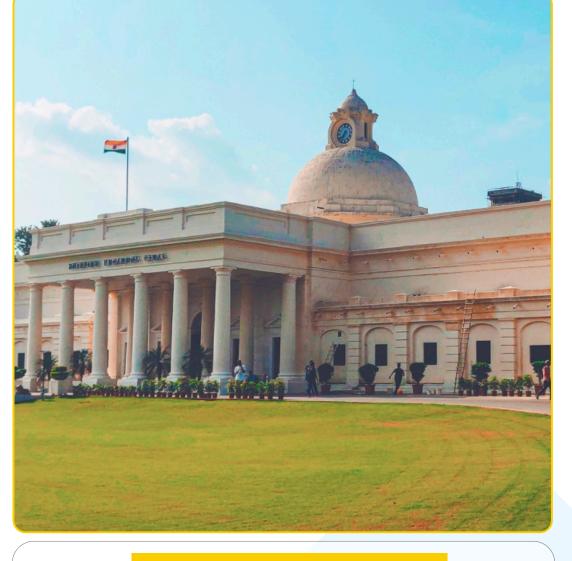## Foundations of VLSI Design Verification

In association with

June 23 – July 14, 2025
Register Before: June 21, 2025

Mode of Delivery is Online

Course Outcomes

- Understand complete VLSI design and verification flow
- Write efficient RTL code and build reusable testbenches
- Apply simulation and debugging techniques using EDA tools
- Use assertions and UVM for scalable verification
- Analyze functional coverage and verification metrics
- Align academic projects with industry verification standards
- Guide students in advanced digital design and verification topics

About E&ICT Academy

Electronics and ICT Academy is an initiative of Ministry of Electronics & Information Technology (MeitY), Govt. of India for conducting various Faculty/ Research Scholar Development Programme. Academy has planned short-term training programs on fundamental and advanced topics in IT, Electronics & Communication, Product Design, and Manufacturing with hands-on training and project work using the latest software tools and systems. In addition, the Academy will conduct specialized/customized training programs and research promotion workshops for corporate sector & educational institutions.

Prerequisites

Basic knowledge of semiconductor physics, electronic circuits, and familiarity with simulation or programming tools.

Experts from Academia/Industry

Who Should Register?

Any Interested Faculty/PhD-Scholars UG/PG/ & Industry Persons can register

Registration Fee

Fees: ₹ 500/- Faculty/Research Scholar/ Students
₹ 1000/- Industry/Others
Note: Refund will be done in case of course cancellation only, with in 20 working days

How to make Payment

Please make the payment first using the below link upload the payment receipt when filling out the Google registration form.

https://eict.iitr.ac.in/instruction-for-payment/

Conference Code: EICTIITR-JFDP-NKN-05

Registration Link

https://forms.gle/7Mp8SgGYuTviPJkp6

Scan QR for registration
Register before: June 21, 2025

Click on icon to follow us on:

Objectives of the course

- To introduce the fundamentals of VLSI design and verification methodologies.
- To enhance understanding of RTL design, logic synthesis, and simulation.
- To explore formal and functional verification techniques and their applications.
- To familiarize faculty with industry-standard tools and languages (SystemVerilog, UVM).
- To bridge academic learning with industry practices and real-time projects.
- To develop skills for debugging, coverage analysis, and testbench design.
- To prepare faculty for guiding student research in VLSI and embedded systems.

Focus Areas

- VLSI design flow: RTL to GDSII
- HDL coding (Verilog/SystemVerilog) and best practices
- Simulation and testbench architecture
- Functional and formal verification techniques
- Assertion-based verification and UVM methodology
- Design coverage, debug, and verification planning
- Industrial EDA tools and case studies

Course Features

- 40 Hours of Lectures, Hands-on, and Pedagogy/Industry sessions.
- Lectures from Expert Speakers, Hands-on from industry/Academia experts.
- Access to learning material and video lectures
- Certificate by E&ICT Academy IIT Roorkee

Principal Coordinator

- Dr. Vineet Sahula, MNIT Jaipur

Joint Principal Coordinator

- Prof. Sanjeev Manhas, IIT Roorkee
- Prof. Anand Bulusu, IIT Roorkee
- Dr. J Ghosh & Dr. Rajeev Arya, NIT Patna
- Dr. Dip Prakash Samajdar , IIITDM Jabalpur

Reach Us:

- M.No.: 8112766397
- Landline No.: +91-1332286457
- Email: eict@iitr.ac.in